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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/499,599	02/07/00	AOKI	Y 00068/LH

EXAMINER	
TRAN, T	
ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 11/07/01

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due Feb 7 02

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

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Office Action Summary	Application No.	Applicant(s)	
	09/499,599	AOKI ET AL.	
	Examiner	Art Unit	
	THANH V TRAN	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *20 Aguqust 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18 and 19-23(newly added)* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18 and 19-23 (newly added)* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15)☒ Notice of References Cited (PTO-892)
16)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17)☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
18)☐ Interview Summary (PTO-413) Paper No(s). _____ .
19)☐ Notice of Informal Patent Application (PTO-152)
20)☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 and 3 are rejected under 35 U.S.C 102 (b) as being anticipated by Mihara et al. (U.S. patent # 6,140,155).

Referring to the figure 12b, Mihara et al. disclose a semiconductor substrate 41 having a circuit element formation region and a plurality of connection pad, the plurality of connection pad 44 including:

At least one first connection pad 44 connected to a barrier layer 45 provided on the circuit element formation region, through a first insulating film interposed therebetween 42, the circuit element formation region and which is electrically connected to at least one first straight –shaped columnar electrode 47, and at least one second connection pad 44 electrically connected to a second conductor layer 46 on the barrier layer 45, and the second conductor layer being connected to at least one second straight-shaped columnar electrode 47.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mihara et al in view of Koshsiek (previous applied).

Mihara et al. show most aspects of the instant invention (paragraph 2) but does not show a barrier layer including one of ground potential layer, a power supply potential layer and an electromagnetic wave absorption layer. In figure 2, Koshsiek shows conductor track 3 is connected at a suitable point to the ground (column 2, lines 13, 14). The motivation for doing so would have been provide a metal layer which is connected to ground potential and covers the whole surface in order to avoid a cross-talk between the conductor tracks of the two aforementioned wiring levels (column 1,lines 39 to 42).

It would be obvious to one of ordinary skill in the art to combine the ground potential layer to the semiconductor device of Mihara et al. as taught by Koshsiek to avoid cross-talk.

4. Claim 4 is rejected under 35 U.S C 103 (a) as being uppatentable over Mihara et al. in view of Suzuki et al.(previous applied).

Mihara et al. show most aspects of the instant invention (paragraph 2) but do not show the planar circuit element adhered to the lower surface of the semiconductor substrate. In figure 10, Suzuki et al. disclose attaching the circuit component 13 to the lower substrate 11. The purpose of doing this would have been to transfer the heat generated in the circuit component to the mother board without passing through the substrate (column 1, lines, 66-67 to column 2, line 1). It would be obvious to one of

ordinary skill in the art to modify the semiconductor device of Mihara et al. by attaching a circuit component to the lower surface of semiconductor substrate as taught by Suzuki et al. to transfer the heat generated in the circuit component to the mother board without passing through the substrate.

5. Claim 5 is rejected under 35 U.S C 103 (a) as being uppatentable over Mihara et al. in view of Suzuki et al. and further in view of Noma et al. (U.S patent # 5,818,079, previous applied).

Mihara et al. in view of Suzuki et al. show most aspects of the instant invention (paragraph 4) but do not disclose the planar circuit element including one of a film-like capacitor and a film-like resistor. Noma et al. teach a semiconductor device having a thin- film capacitor with the lower electrode 53A, the upper electrode 55A, and a capacity insulating film 54A (column 1, lines 55,56,61 and 62). The purpose for doing so would have provided a high integration of the semiconductor integrated circuit device, the chip area have been reduced by the high integration in order to get small-sized information communication equipment and to lower the cost (Column 1, line 18-21). It would be obvious to one of ordinary skill in the art to form a thin- film capacitor in the semiconductor device of Mihara et al. in view of Suzuki et al. as taught by Noma et al. to get small- sized information communication equipment and to lower the cost.

6. Claims 6,8 ,13 and 19-23 (newly added) are rejected under 35 U.S.C. 103(a) as being unpatentable over Mihara et al. in view of Brotherton. (previous applied).

Mihara et al. show most aspects of the instant invention (paragraph 2) but do not show a thin-film circuit element provided on the first insulating film. Referring to

figure 3, Brotherton discloses forming a thin- film circuit elements 36 having a conductive layer 1 with a insulating film 3 interposed (column 5, lines 19-20). The motivation of doing so have been desired for high mobility, for example for fast switching applications, crystsalline semiconductor regions (column 1, lines 29-30) It would be obvious to one of ordinary skill in the art to form a thin- film element provided on the first insulating film of semiconductor device of Mihara et al. as taught by Brotherton where high mobility is desired.

Examiner notes that it is obvious to duplicate the first barrier layer in the semiconductor device of the instant invention to get the second barrier layer as claimed in claim 13 to increase the capacity of semiconductor device.

7. Claims 7 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mihara et al. in view of Brotherton , and further in view of Kohsiek .

Mihara et al. in view of Brotherton show most aspects of the instant invention (paragraph 6) but do not show a barrier layer including one of a ground potential layer, a power supply potential layer and an electromagnetic wave absorption layer. In figure 2, Koshsiek shows conductor track 3 is connected at a suitable point to the ground (column 2, lines 13, 14). The motivation for doing so would have been provided a metal layer which is connected to ground potential and covers the whole surface in order to avoid a cross-talk between the conductor tracks of the two aforementioned wiring levels (column 1,lines 39 to 42). It would be obvious to one of ordinary skill in the art to combine the ground potential layer to the semiconductor device of Mihara et al. in view

of Brotherton as taught by Koshsiek to avoid a cross-talk between the conductor tracks of the two aforementioned wiring levels.

8. Claims 10 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mihara et al. in view of Brotherton as applied to the claim 6 above , and further in view of Noma et al.

Mihara et al. in view of Brotherton show most aspects of the instant invention (paragraph 6) but do not show a thin- film circuit element including one of a thin- film inductor, a thin- film transformer, a thin-film capacitor, a thin –film SAW filter, a microstrip line, and a MMIC (Microwave Monolithic Integrated Circuit). In figure 11, Noma et al. teach a semiconductor device having a thin- film capacitor with the lower electrode 53A, the upper electrode 55A, and a capacity insulating film 54A (column 1, lines 55,56,61 and 62). The purpose for doing so would have provided a high integration of the semiconductor integrated circuit device, the chip area have been reduced by the high integration in order to get small- sized information communication equipment and to lower the cost (Column 1, line 18- 21). It would be obvious to one of ordinary skill in the art to form a thin- film capacitor to the semiconductor device of Mihara et al. in view of Brotherton as taught by Noma et al. to get small- sized information communication equipment and to lower the cost.

9. Claims 11 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mihara et al. in view of Brotherton as applied to claim 6 above, and further in view of Suzuki.

Mihara et al. in view of Brotherton show most aspects of the instant invention (paragraph 6) but do not show a planar circuit element adhered to the lower surface of the semiconductor substrate. In figure 10, Suzuki et al. disclose attaching the circuit component 13 to the lower substrate 11. The purpose of doing this would have been to transfer the heat generated in the circuit component to the mother board without passing through the substrate (column 1, lines, 66-67 to column 2, line 1). It would be obvious to one of ordinary skill in the art to modify the semiconductor device of Mihara et al. in view of Brotherton by attaching a circuit component to the lower surface of semiconductor substrate as taught by Suzukii et al. to transfer the heat generated in the circuit component to the mother board without passing through the substrate.

10. Claims 12 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mihara et al. in view of Brotherton and Suzuli et al. as applied to claim 11 above, and further in view of Noma et al.

Mihara et al. in view of Brotherton and Suzuki et al. show most aspects of the instant invention (paragraph 9) but do not show the planar circuit element including one of a film-like capacitor and a film-like resistor. Noma et al. teach a semiconductor device having a thin- film capacitor with the lower electrode 53A, the upper electrode 55A, and a capacity insulating film 54A (column 1, lines 55,56,61 and 62). The purpose for doing so would have provided a high integration of the semiconductor integrated circuit device, the chip area have been reduced by the high integration in order to get small- sized information communication equipment and to lower the cost (Column 1, line 18- 21). It would be obvious to one of ordinary skill in the art to add a

thin- film capacitor to the semiconductor device of Mihara et al. in view of Brotherton and Suzuki et al. as taught by Noma et al. to provide a high integration of semiconductor circuit and get small- sized information communication equipment and to lower the cost.

Response to Arguments

11. Applicant's arguments with respect to claims 1-18 and 19-23(newly added) have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

12. Papers related to this application may be submitted directly to Art Unit 2814 by facsimile transmission. Papers should be fax to Art Unit 2814 via the Art Unit 2814 Fax Center located in Crystal Plaza 4, room 4C23. The faxing of such papers must conform with the notice published in the official Gazette,1096 OG 30(15 November 1989). The Art Unit 2814 Fax Center number is (703)308-7722 or –7724. The Art Unit 2824 Fax Center is to be used only for papers related to Art Unit 2814 applications.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to THANH V TRAN whose telephone number is 703-306-0208. The examiner can normally be reached on 8:00AM-5:00PM Monday through Friday or by e-mail via Thanh.Tran@uspto.gov.

14. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chuadhuri can be reached on 703-306 2794. The fax phone numbers for the organization where this application or proceeding is assigned

are 703 -308-7722 for regular communications and 703 -305-3431 for After Final communications.

15. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

16. The following list is the Examiner's field of search for the present Office Action:

Field of Search	Date
U.S Class/Subclass(es): 257/734,532,536,758,753,759,760,748,508 438/957,382,118,622,348,361	11/04/01
Other Documentation: none	
Electronic Database(s): WEST(USPAT)	11/04/01

Thanh Tran
November 4, 2001

OLIK CHAUDHURI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Notice of References Cited	Application/Control No. 09/499,599	Applicant(s)/Patent Under Reexamination AOKI ET AL.	
	Examiner THANH V TRAN	Art Unit 2814	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification	
	A	US-6140155-	10-2000	Mihara et al.	438	124
	B	US- -				
	C	US- -				
	D	US- -				
	E	US- -				
	F	US- -				
	G	US- -				
	H	US- -				
	I	US- -				
	J	US- -				
	K	US- -				
	L	US- -				
	M	US- -				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification	
	N	- -					
	O	- -					
	P	- -					
	Q	- -					
	R	- -					
	S	- -					
	T	- -					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.